semiconductor substrate, a patterned hard mask nitride layer exposing portions of said substrate so as to define an isolation region;

SUB C1

b. etching exposed portions of said substrate using said patterned hard mask nitride layer to form an isolation trench in the isolation region;

B1

c. oxidizing said substrate to form a thermal oxide layer in [an] said isolation trench and capacitor trench;

d. depositing an oxide layer over the thermal oxide layer to fill unfilled portions of [the] said isolation trench;

e. removing said patterned hard mask nitride layer;

f. planarizing said substrate and forming a pad nitride strip;

II) forming a sacrificial gate oxide layer in areas of the semiconductor substrate surface where [the] said pad nitride has been stripped;

III) affecting channel implants in selected areas using resist masks;

IV) affecting a first low dose angled nitrogen implant without using an implant mask to limit the nitrogen dose in the active area to the inner part of the gate area so that the nitrogen dose in the shadow area of the active area is less than the amount of the nitrogen dose

implanted in the remaining non-shadowed area to cause spatial thickness distribution of all exposed oxide areas;

V) affecting masking so that nitrogen ions (N_2^+) to be implanted do not penetrate the masked region; and

VI) affecting a second nitrogen ion implantation by employing a shadow area inducing means at a temperature sufficient to provide a lesser amount of nitrogen ion dosage in the inner part of the gate area so that the angled nitrogen in the shadow area of the active area is less than the amount of nitrogen dose implanted in the remaining non-shadowed area.

2. (Twice Amended) The process of claim 1 wherein said shadow area inducing means is by angled nitrogen ion implantation at an angle either greater or less than 90° with respect to the surface normal of said semiconductor substrate.

CORRECTED VERSION OF THE AMENDED CLAIMS

1. In a process for forming dual gate oxides for use in high performance DRAM systems or logic circuits, the improvement comprising using a shadow area to control gate oxide thickness at active area (AA) corners adjacent a shallow trench isolation (STI) region, comprising:

I) a. forming an active area by depositing over a semiconductor substrate, a patterned hard mask nitride layer exposing portions of said substrate so as to define an isolation region;

b. etching exposed portions of said substrate using said patterned hard mask nitride layer to form an isolation trench in the isolation region;

c. oxidizing said substrate to form a thermal oxide layer in said isolation trench and capacitor trench;

d. depositing an oxide layer over the thermal oxide layer to fill unfilled portions of said isolation trench;

e. removing said patterned hard mask nitride layer;

f. planarizing said substrate and forming a pad nitride strip;

II) forming a sacrificial gate oxide layer in areas of the semiconductor substrate surface where said pad nitride has been stripped;

III) affecting channel implants in selected areas using resist masks;

IV) affecting a first low dose angled nitrogen implant without using an implant mask to limit the nitrogen dose in the active area to the inner part of the gate area so that the nitrogen dose in the shadow area of the active area is less than the amount of the nitrogen dose implanted in the remaining non-shadowed area to cause spatial thickness distribution of all exposed oxide areas;

V) affecting masking so that nitrogen ions (N_2^+) to be implanted do not penetrate the masked region; and

VI) affecting a second nitrogen ion implantation by employing a shadow area inducing means at a temperature sufficient to provide a lesser amount of nitrogen ion dosage in the inner part of the gate area so that the angled nitrogen in the shadow area of the active area is less than the amount of nitrogen dose implanted in the remaining non-shadowed area.

2. The process of claim 1 wherein said shadow area inducing means is by angled nitrogen ion implantation at an angle either greater or less than 90° with respect to the surface normal of said semiconductor substrate.